REMARKS

Upon entry of the instant Amendment, Claims 1-10, 12, 14, and 19-20 are pending. Claims 5, 12, and 14 have been amended to more particularly point out Applicant's invention.

Claims 4, 8, and 19 have been rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject mater which applicant regards as the invention.

In particular, the limitations in claims 4, 8, and 19 of "said second clock frequency comprising a frame clock rate" was indicated to be "unclear" because "it is not understood how a clock/frequency can comprise another clock frequency, as the frequencies which are interrelated, as being multiples of the same source frequency, do not comprise each other or the source frequency..." Applicant does not understand the basis for this rejection. The term "multiple" does not appear in Applicant's Specification. A clock frequency may comprise, for example, any clocking rate (thus the Patent Office's apparent reading of particular values into that recitation is inappropriate). The limitation in question simply specifies that the particular clock frequency (the second) may be of a frame clock rate. The limitations are thus believed to be clear. However, if the Patent Office maintains the rejection, the Examiner is requested to provide evidence that the recited claim language would, in fact, be unclear to a person of ordinary skill in the art.

Claims 1-10, 12, 14, and 19-20 have been rejected under 35 U.S.C. 103 as being unpatentable over Greenblatt, U.S. Patent No. 5,136,586 ("Greenblatt") in view of Matsumoto, U.S. Patent No. 5,812,944 ("Matsumoto"). Applicants respectfully submit that the claimed invention is not taught, suggested or implied by Greenblatt or Matsumoto, either singly or in combination.

As discussed in the Specification, and in response to the previous Official Action, the present invention relates to a system and method for rate adjustment and jitter buffering. A rate adjustment system according to an embodiment of the invention includes a first jitter buffer pair and a second buffer pair. The buffers in the first and second jitter buffer pairs are swapped to effect a rate adjustment. In particular, the buffers in the pairs are alternately filled at a first clock rate and emptied at a second. The swapping occurs

simultaneously at the second clock rate. In some embodiments, the first clock is associated with a sample clock frequency and the second clock is associated with a frame clock frequency.

Claims 1 and 19 thus each recite first and second clock domains, as well as pairs of jitter buffers that interface between the first and second clock domains, i.e., domains of different clock sources. As discussed in the Specification, one clock domain may, for example, be a local clock and the second may be from a different clock source, and even remotely derived.

In contrast, while Greenblatt provides a clock C and a clock C2, these are not from first and second domains, as recited in the claims at issue. Indeed, these are both sample clocks (the clock C samples voice V and the clock C2 samples voice V') and are derived from a single clock source and therefore single domain. The Examiner's attention is directed to FIG. 5 of Greenblatt, in which a single "high speed system clock" is divided into clocks C and C2. Because Greenblatt does not provide first and second clock domains, Greenblatt also does not provide pairs of jitter buffers that interface between such domains.

Paragraph 10 of the Official Action acknowledges that clocks C and C2 are derived from the same clock, yet maintains that these are different domains. While the Patent Office is entitled to a broad interpretation of claims, it is not entitled to one that is illogical or contradicts the understanding of a person of ordinary skill in the art. Indeed, the Patent Office provides no basis whatsoever for the assertion that applicant's first and second domains would be interpreted as being derived from a same clock or that the recitation would ever be understood as such by a person of ordinary skill in the art.

Matsumoto is relied on for allegedly teaching a bi-directional wireless system. However, Matsumoto does not teach, suggest, or imply, that pairs of jitter buffers interfacing across different clock domains can be alternated, as generally recited in the claims at issue. As such, the Examiner is respectfully requested to reconsider and withdraw the rejection.

The remaining claims have been amended to recite, in claim 5, "wherein said first or second jitter buffers alternately fill at a first clock frequency and empty at a second clock frequency, wherein alternation between said first and second jitter buffers occurs at said second clock frequency; wherein said third or fourth jitter buffers alternately fill at said

second clock frequency and empty at said first clock frequency, wherein alternation between said third and fourth jitter buffers occurs simultaneously with said alternation between said first and second jitter buffers at said second clock frequency, said first clock frequency associated with a sample clock in a first clock domain, said second clock frequency associated with a frame clock in a second clock domain external the first clock domain;" in claim 12, "switching between using said first or second jitter buffers at said second clock rate; and switching between using said third or fourth jitter buffers simultaneously with said switching between using said first or second jitter buffers at said second clock rate, said first clock rate being associated with a sample clock in a first clock domain, said second clock rate being associated with a frame clock in a second clock domain external the first clock domain;" and in claim 14, "receiving at first or second jitter buffers a plurality of samples at a first clock rate and transmitting a block of said samples at a second clock rate; and switching between using said first or second jitter buffers at said second clock rate; receiving at third or fourth jitter buffers blocks of samples at said second clock rate and transmitting a plurality of samples at said first clock rate; and switching between using said third or fourth jitter buffers simultaneously with said switching between using said first or second jitter buffers at said second clock rate, said first clock rate being a sample clock rate in a first clock domain, said second clock rate being a frame clock rate in a second clock domain external the first clock domain."

Thus, these claims, too, have been amended to recite first and second clock domains and further that the second is external the first clock domain. For reasons similar to those discussed above, these claims, too, are believed allowable. As such, the Examiner is respectfully requested to reconsider and withdraw the rejection.

For all of the above reasons, Applicants respectfully submit that the application is in condition for allowance, which allowance is earnestly solicited.

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